AMENDMENTS TO THE DRAWINGS:

Responsive to the Examiner's requirement that Figures 1-4b should be designated by a legend such as --Prior Art--, corrected drawings in compliance with 37 CFR 1.121(d) are submitted herewith.

Responsive to the Examiner's determination that the drawings fail to comply with 37 CFR 1.84(p)(4), Applicants propose amending drawing Figures 15, as set forth below.

Regarding Figure 1, Applicants propose changing the identifier "100" to instead be "101" so as to avoid confusion.

Applicants respectfully request approval.

REMARKS/ARGUMENT

1) Claims 1-10 and 18-27 stand rejected under 35 U.S.C. 102(b) as being anticipated by Rasmussen et al (US Patent No. 5,732,106). Applicants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claims 1-10 and 18-27 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." Verdegall Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 1 requires and positively recites, a transmit filter for generating an oversampled signal from a stream of data symbols generated responsive to a symbol clock, comprising: "circuitry for receiving the data symbol stream" , "**phase tracking circuitry**, responsive to a reference clock generated independently from the symbol clock, **for maintaining phase information relative to the symbol clock**" and "sample generating circuitry for generating samples responsive to said phase information".

Independent Claim 18 requires and positively recites, a method of generating a oversampled signal from a stream of data symbols generated responsive to a symbol clock, comprising the steps of: "receiving the data symbol stream", "**maintaining phase**

information relative to the symbol clock in response to a reference clock generated independently from the symbol clock" and "generating samples responsive to said phase information and said reference clock".

In contrast, Rasmussen (US 5,732,106) discloses "an all digital design to provide pulse shaping of digital input data (...) for RF modulated transmission." The input serial data of low rate, such as 20 kb/s, is oversampled and processed at a higher clock (CLK1) rate, such as 400 kHz. The data is first de-metastabilized and conditioned by the 3:1 majority logic decoder 21 and the data edge detector 24 (column 3 lines 6—49). The up/down counter circuit 26 and the raised cosine decoder 28 serve to turn the sharp positive and negative transitions of the digital input data into gradual transitions (i.e., band limited) at the RF modulator input. The spectral band limiting through edge pulse shaping is illustrated in Figures 4D—4F.

While Rasmussen discloses a non-overflowing up/down counter 26 that is designed to saturate its count after almost every transition, as illustrated in Figure 4E, this saturation feature breaks the counting continuity and loses track of the phase. As such, this feature cannot be referred to as "phase tracker circuitry", as required by Claim 1. The up/down counter merely counts the clocks from the previous data transition so it cannot be used "for maintaining phase information relative to the symbol clock", as required by Claims 1 and 18. As such, Rasmussen fails to teach or suggest, "**phase tracking circuitry**, responsive to a reference clock generated independently from the symbol clock, **for maintaining phase information relative to the symbol clock**", as required by Claim 1 or, "**maintaining phase information relative to the symbol clock** in response to a reference clock generated independently from the symbol clock", as required by Claim 18. Accordingly, the 35 U.S.C. 102(b) rejection of Claims 1 and 18 is overcome.

Indeed, Applicants submit that the distinction between Applicants' claimed invention and that of Rasmussen becomes even more clear when specifically examining the teachings of each specification. Applicants' specification discloses, "the phase tracking circuit 106 determines a position in the output relative to a hypothetical baseband clock." (Paragraph [0050]). The example in Figure 5 shows a non-integer ratio of the available clock frequency or rate (2.25 MHz) to the symbol rate (1 Mb/s). The phase of the clock and the symbol are synchronized at the timing origin. The symbol transitions do not coincide or have a fixed relationship with the data transitions but their separation is constantly changing. It is the function of the phase tracking circuit to maintain the phase of the data transitions from the timing origin. The phase tracking circuit in Figure 8a, and described in Paragraphs [0055] and [0056], is constructed as a fixed-point (non-integer number) overflowing accumulator.

Contrast the above with Rasmussen's specification which discloses only a specific ratio (400 kHz / 20 kb/s) of the higher rate CLK1 clock and the input data rate. While this ratio can take on different values for various realizations, it is substantially fixed for a given realization. Rasmussen does not teach or suggest programmability of that ratio that would allow one to support different data rates and/or different clock frequencies. Rasmussen merely suggests adjusting the number of bits of the up/down counter depending on the sampling rate (column 4 lines 5—8). Similarly, Rasmussen's invention will not operate for non-integer values of the ratio of the data rate to the clock rate. Rasmussen does not teach or suggest an arbitrary data rate or arbitrary clock rate. Finally, the modulation scheme disclosed in Rasmussen is not bandwidth efficient since the circuit does not allow for any modern modulation schemes that would allow a controllable amount of intersymbol-interference (ISI) that would maximize ratio of the data rate to the occupied RF bandwidth. The ISI support requires memory of the previous bits or symbols (states), which Rasmussen does not teach or suggest.

Claims 2-10 and 19-27 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 2 further defines the transmit filter of claim 1 wherein said sample generating circuitry generates samples at an active edge of said reference clock. Claim 2 depends from Claim 1 and is therefore allowable for the same reasons set forth above for the allowance of Claim 1.

Claim 3 further defines the transmit filter of claim 2 wherein said sample generating circuitry generates samples on each clock cycle of said reference clock. Claim 3 depends from Claim 2 and is therefore allowable for the same reasons set forth above for the allowance of Claim 2.

Claim 4 further defines the transmit filter of claim 2 wherein said sample generating circuitry generates samples on selected clock cycles of said reference clock. Claim 4 depends from Claim 2 and is therefore allowable for the same reasons set forth above for the allowance of Claim 2. Moreover, and contrary to the Examiner's assertion, Rasmussen does not teach or suggest "generating samples on selected clock cycles of said reference clock." Column 4, lines 44—47 describes generating samples on ALL clock cycles of the reference clock (CLK1, which is generated by the timing and control circuit 29 in response to the NCO clock 17 output).

Claim 5 further defines the transmit filter of claim 1 wherein said reference clock comprises the output of a frequency divider. Claim 5 depends from Claim 1 and is therefore allowable for the same reasons set forth above for the allowance of Claim 1. Moreover, and contrary to the Examiner's assertion, Rasmussen does not teach or suggest "said reference clock comprises the output of a frequency divider." The text in column 4,

lines 5—8 merely refers to the definition of the sampling rate being the ratio of the clock rate to the input data rate.

Claim 6 further defines the transmit filter of claim 1 wherein said reference clock is selectable from two or more clock signals. Claim 6 depends from Claim 1 and is therefore allowable for the same reasons set forth above for the allowance of Claim 1. Moreover, and contrary to the Examiner's assertion, Rasmussen does not teach or suggests that "said reference clock is selectable from two or more clock signals". The text in column 3, lines 11--14 describes only one fixed and non-selectable clock source of 400 kHz frequency.

Claim 7 further defines the transmit filter of claim 1 wherein said phase tracking circuitry comprises circuitry for adding a predetermined value to a stored value on each clock cycle of said reference clock. Claim 7 depends from Claim 1 and is therefore allowable for the same reasons set forth above for the allowance of Claim 1.

Claim 8 further defines the transmit filter of claim 7 wherein said predetermined value is a ratio between a frequency associated with said symbol clock and a frequency associated with said reference clock. Claim 8 depends from Claim 7 and is therefore allowable for the same reasons set forth above for the allowance of Claim 7.

Claim 9 further defines the transmit filter of claim 1 and further comprising circuitry for storing a current data symbol and a predetermined number of preceding data symbols. Claim 9 depends from Claim 1 and is therefore allowable for the same reasons set forth above for the allowance of Claim 1.

Claim 10 further defines the transmit filter of claim 9 wherein said sample generating circuitry comprises circuitry for generating a sample point responsive to said phase information, said current data symbol and one or more of said preceding data symbols. Claim 10 depends from Claim 9 and is therefore allowable for the same reasons set forth above for the allowance of Claim 9. Moreover, and contrary to the Examiner's assertion, Rasmussen does not teach or suggests a "circuitry for generating a sample point responsive to said phase information ..." Figure 3 (block 21) only generates the up/down signal and does not generate sample points, which are generated by the raised cosine decoder 28. In addition, Figure 3 is not responsive to the phase information, which does not appear in Rasmussen.

Claim 11 further defines the transmit filter of claim 10 wherein symbol data for generating a sample point is defined by a plurality of transfer function curves. Claim 11 depends from Claim 10 and is therefore allowable for the same reasons set forth above for the allowance of Claim 10.

Claim 12 further defines the transmit filter of claim 11 wherein symbol data for one of said curves is stored in a memory and symbol data for other of said curves is derived from said symbol data for said one curve. Claim 12 depends from Claim 11 and is therefore allowable for the same reasons set forth above for the allowance of Claim 11.

Claim 13 further defines the transmit filter of claim 11 wherein the symbol data for said one curve comprises a power of two number of data points. Claim 13 depends from Claim 11 and is therefore allowable for the same reasons set forth above for the allowance of Claim 11.

Claim 14 further defines the transmit filter of claim 11 wherein said memory stores symbol data for multiple sets of transfer curves. Claim 14 depends from Claim 11 and is therefore allowable for the same reasons set forth above for the allowance of Claim 11.

Claim 15 further defines the transmit filter of claim 11 wherein symbol data for multiple sets of transfer curves are stored in respective memories. Claim 15 depends from Claim 11 and is therefore allowable for the same reasons set forth above for the allowance of Claim 11.

Claim 16 further defines the transmit filter of claim 1 and further comprising circuitry for identifying an approximate center of a data symbol. Claim 16 depends from Claim 1 and is therefore allowable for the same reasons set forth above for the allowance of Claim 1.

Claim 17 further defines the transmit filter of claim 16 and further comprising circuitry for tracking an approximate center for each data symbol in said stream independent of the symbol clock. Claim 17 depends from Claim 16 and is therefore allowable for the same reasons set forth above for the allowance of Claim 16.

Claim 19 further defines the method of claim 18 wherein said sample generating step comprises the step of generating samples at an active edge of said reference clock. Claim 19 depends from Claim 18 and is therefore allowable for the same reasons set forth above for the allowance of Claim 18.

Claim 20 further defines the method of claim 19 wherein said sample generating step comprises the step of generating samples on each clock cycle of

said reference clock. Claim 20 depends from Claim 19 and is therefore allowable for the same reasons set forth above for the allowance of Claim 19.

Claim 21 further defines the method of claim 19 wherein said sample generating step comprises the step of generating samples on selected clock cycles of said reference clock. Claim 21 depends from Claim 19 and is therefore allowable for the same reasons set forth above for the allowance of Claim 19. Moreover, and contrary to the Examiner's assertion, Rasmussen does not teach or suggest "generating samples on selected clock cycles of said reference clock." Column 4, lines 44—47 describes generating samples on ALL clock cycles of the reference clock (CLK1, which is generated by the timing and control circuit 29 in response to the NCO clock 17 output).

Claim 22 further defines the method of claim 18 and further comprising the step of generating the reference clock through a frequency divider. Claim 22 depends from Claim 19 and is therefore allowable for the same reasons set forth above for the allowance of Claim 18. Moreover, and contrary to the Examiner's assertion, Rasmussen does not teach or suggest "said reference clock comprises the output of a frequency divider." The text in column 4, lines 5—8 merely refers to the definition of the sampling rate being the ratio of the clock rate to the input data rate.

Claim 23 further defines the method of claim 18 and further comprising the step of selecting the reference clock from two or more clock signals. Claim 23 depends from Claim 18 and is therefore allowable for the same reasons set forth above for the allowance of Claim 18. Moreover, and contrary to the Examiner's assertion, Rasmussen does not teach or suggests that "said reference clock is selectable from two or more clock

signals". The text in column 3, lines 11--14 describes only one fixed and non-selectable clock source of 400 kHz frequency.

Claim 24 further defines the method of claim 18 wherein said step of maintaining phase information comprises the step of adding a predetermined value to a stored value on each clock cycle of said reference clock. Claim 24 depends from Claim 18 and is therefore allowable for the same reasons set forth above for the allowance of Claim 18.

Claim 25 further defines the method of claim 24 wherein said predetermined value is a ratio between a frequency associated with said symbol clock and a frequency associated with said reference clock. Claim 25 depends from Claim 24 and is therefore allowable for the same reasons set forth above for the allowance of Claim 24.

Claim 26 further defines the method of claim 18 and further comprising the step of storing a current data symbol and a predetermined number of preceding data symbols. Claim 26 depends from Claim 18 and is therefore allowable for the same reasons set forth above for the allowance of Claim 18.

Claim 27 further defines the method of claim 26 wherein said sample generating step comprises the step of generating a sample point responsive to said phase information, said current data symbol and one or more of said preceding data symbols. Claim 27 depends from Claim 26 and is therefore allowable for the same reasons set forth above for the allowance of Claim 26. Moreover, and contrary to the Examiner's assertion, Rasmussen does not teach or suggests a "circuitry for generating a sample point responsive to said phase information ..." Figure 3 (block 21) only generates the up/down signal and does not generate sample points, which are generated by the raised cosine decoder 28. In addition, Figure 3 is not responsive to the phase information, which does not appear in Rasmussen.

2) Claims 34-36 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Rasmussen et al (US Patent No. 5,732,106). Applicants respectfully traverse this rejection, as set forth below.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Moreover, **the mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** In re Gordon, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.** In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 34 requires and positively recites, a transmit filter for generating an oversampled signal from a stream of data symbols generated responsive to a symbol clock, comprising: "circuitry for receiving the data symbol stream" , "**phase tracking circuitry**, responsive to a reference clock, **for maintaining phase information relative to the symbol clock**" and "sample generating circuitry for generating samples responsive to said phase information and said symbol clock".

In contrast, Rasmussen (US 5,732,106) discloses "an all digital design to provide pulse shaping of digital input data (...) for RF modulated transmission." The input serial data of low rate, such as 20 kb/s, is oversampled and processed at a higher clock (CLK1) rate, such as 400 kHz. The data is first de-metastabilized and conditioned by the 3:1 majority logic decoder 21 and the data edge detector 24 (column 3 lines 6—49). The up/down counter circuit 26 and the raised cosine decoder 28 serve to turn the sharp positive and negative transitions of the digital input data into gradual transitions (i.e., band limited) at the RF modulator input. The spectral band limiting through edge pulse shaping is illustrated in Figures 4D—4F.

While Rasmussen discloses a non-overflowing up/down counter 26 that is designed to saturate its count after almost every transition, as illustrated in Figure 4E, this saturation feature breaks the counting continuity and loses track of the phase. As such, this feature cannot be referred to as "phase tracker circuitry", as required by Claim 1. The up/down counter merely counts the clocks from the previous data transition so it cannot be used "for maintaining phase information relative to the symbol clock", as required by Claims 1 and 18. As such, Rasmussen fails to teach or suggest, "**phase tracking circuitry**, responsive to a reference clock, **for maintaining phase information relative to the symbol clock**", as required by Claim 34. Accordingly, the 35 U.S.C. 103(a) rejection of Claim 34 is overcome.

Indeed, Applicants submit that the distinction between Applicants' claimed invention and that of Rasmussen becomes even more clear when specifically examining the teachings of each specification. Applicants' specification discloses, "the phase tracking circuit 106 determines a position in the output relative to a hypothetical baseband clock." (Paragraph [0050]). The example in Figure 5 shows a non-integer ratio of the available clock frequency or rate (2.25 MHz) to the symbol rate (1 Mb/s). The phase of the clock and the symbol are synchronized at the timing origin. The symbol transitions do not coincide or have a fixed relationship with the data transitions but their separation is constantly changing. It is the function of the phase tracking circuit to maintain the phase of the data transitions from the timing origin. The phase tracking circuit in Figure 8a, and described in Paragraphs [0055] and [0056], is constructed as a fixed-point (non-integer number) overflowing accumulator.

Contrast the above with Rasmussen's specification which discloses only a specific ratio (400 kHz / 20 kb/s) of the higher rate CLK1 clock and the input data rate. While this ratio can take on different values for various realizations, it is substantially fixed for a given realization. Rasmussen does not teach or suggest programmability of that ratio that would allow one to support different data rates and/or different clock frequencies. Rasmussen merely suggests adjusting the number of bits of the up/down counter depending on the sampling rate (column 4 lines 5—8). Similarly, Rasmussen's invention will not operate for non-integer values of the ratio of the data rate to the clock rate. Rasmussen does not teach or suggest an arbitrary data rate or arbitrary clock rate. Finally, the modulation scheme disclosed in Rasmussen is not bandwidth efficient since the circuit does not allow for any modern modulation schemes that would allow a controllable amount of intersymbol-interference (ISI) that would maximize ratio of the data rate to the occupied RF bandwidth. The ISI support requires memory of the previous bits or symbols (states), which Rasmussen does not teach or suggest.

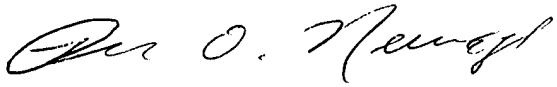
Claims 35 and 36 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 35 further defines the transmit filter of claim the transmit filter of claim 34 wherein said sample generating circuitry generates samples on randomly selected cycles of said reference clock. Claim 35 depends from Claim 34 and is therefore allowable for the same reasons set forth above for the allowance of Claim 34.

Claim 36 further defines the transmit filter of claim the transmit filter of claim 34 wherein said sample generating circuitry generates samples on deterministically selected cycles of said reference clock. Claim 36 depends from Claim 34 and is therefore allowable for the same reasons set forth above for the allowance of Claim 34.

Applicants appreciate the Examiner's determination that Claims 11-17 and 28-33 would be allowable if amended to included the limitations of the base claim and any intervening claims, but believe in light of the above arguments that these claims are allowable in their present form. Claims 1-36 stand allowable over the references of record. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,



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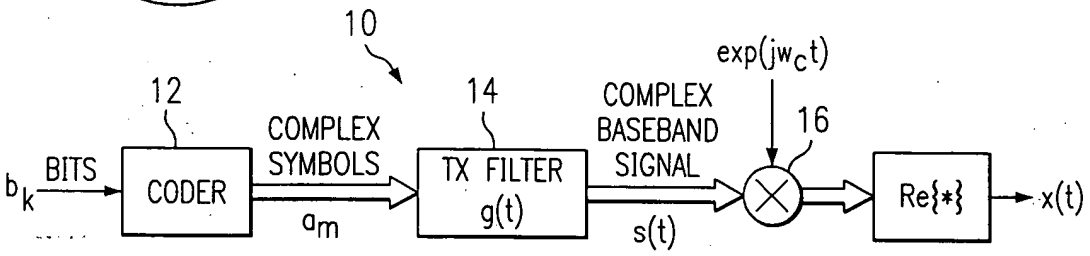


FIG. 1
(PRIOR ART)

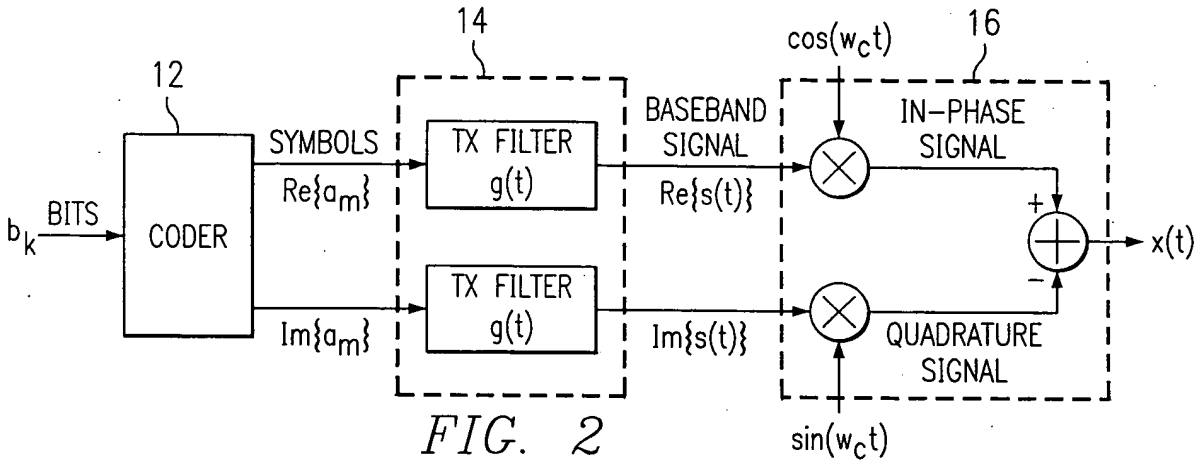


FIG. 2
(PRIOR ART)

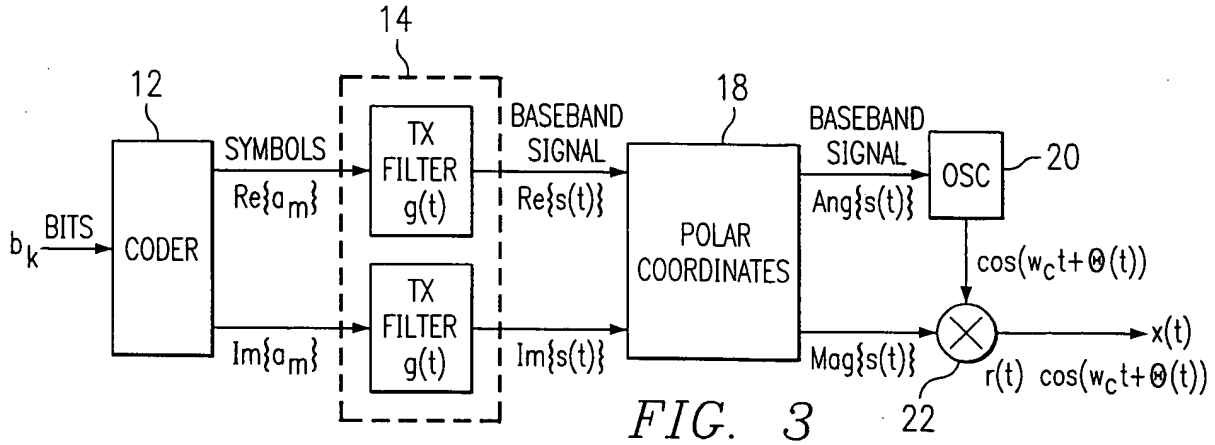


FIG. 3
(PRIOR ART)

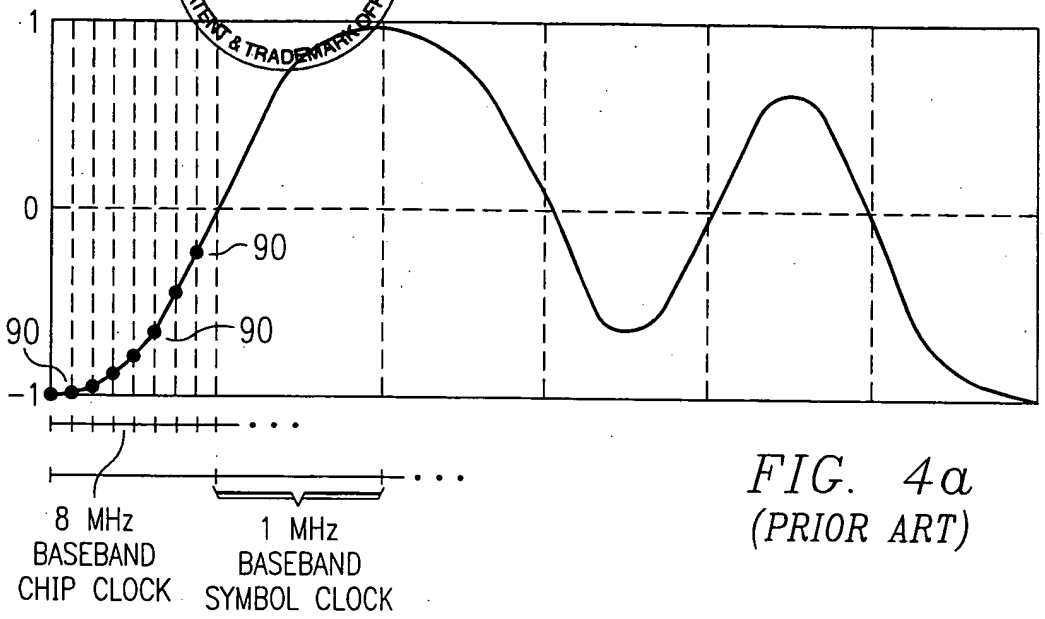


FIG. 4a
(PRIOR ART)

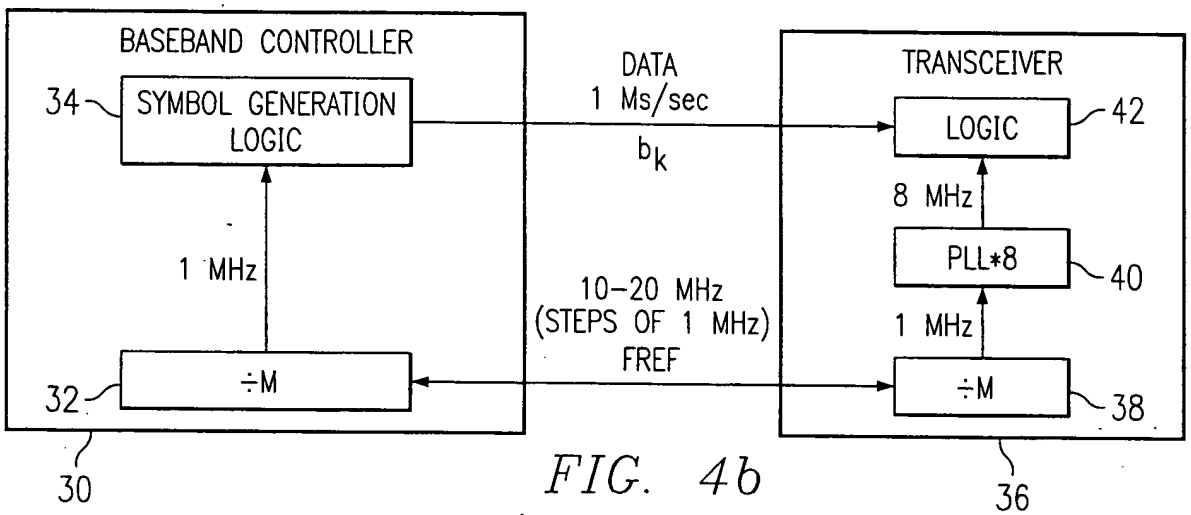


FIG. 4b
(PRIOR ART)

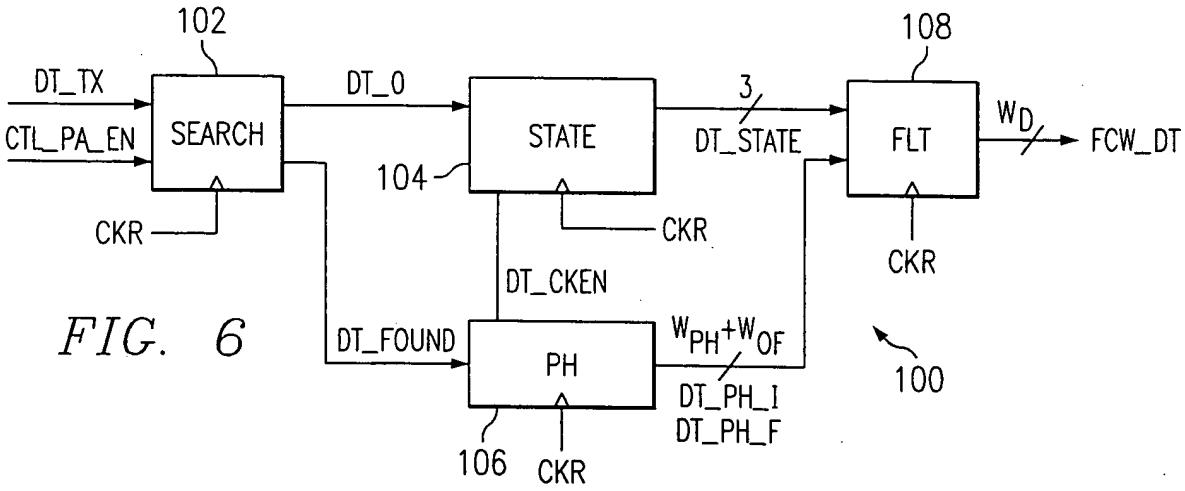
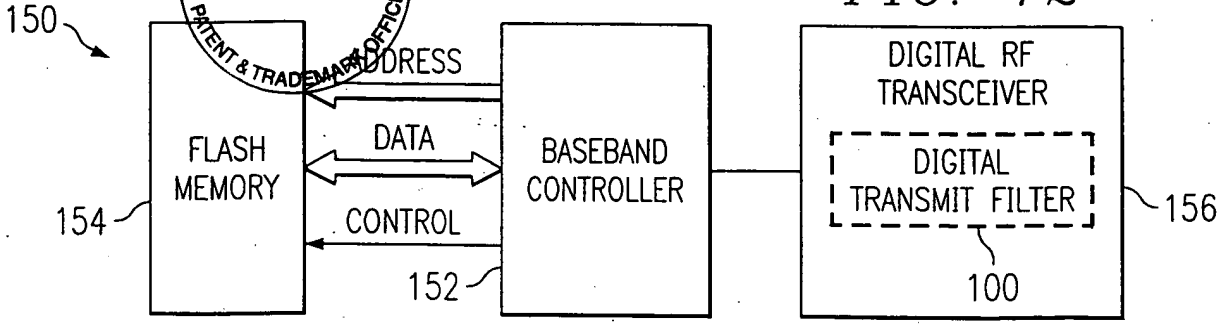


FIG. 6

FIG. 12



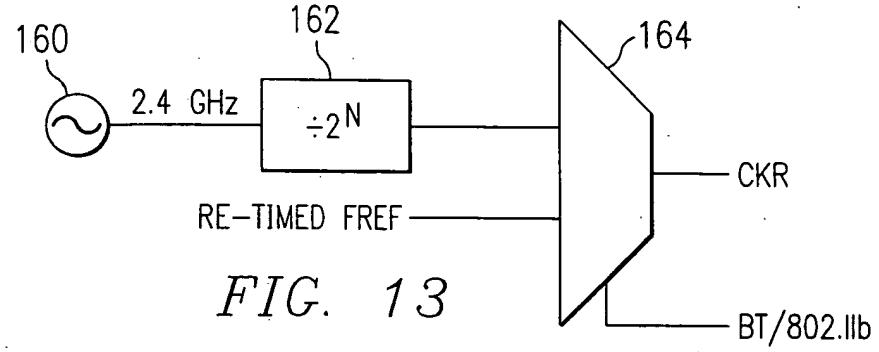


FIG. 13

FIG. 14

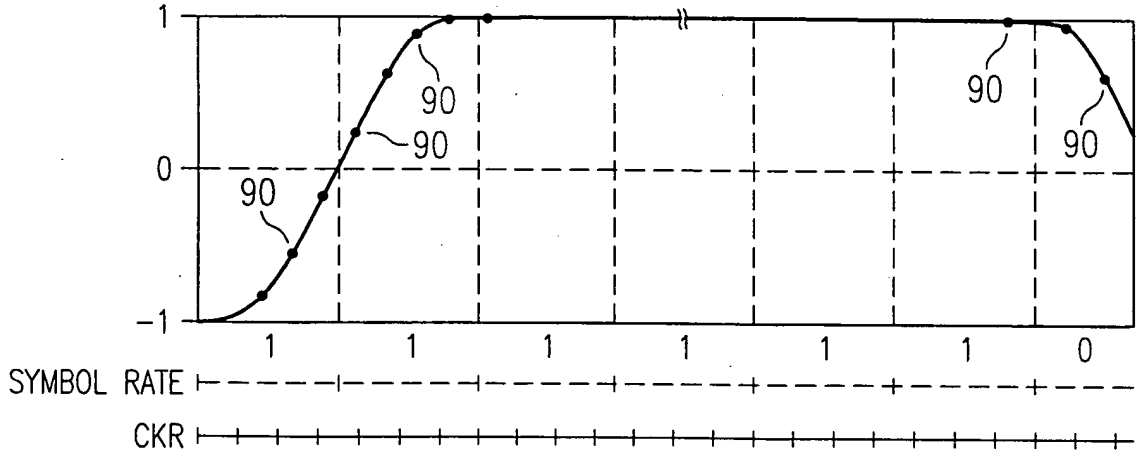


FIG. 15